ESD-TR-76-355, VOLUME I

DETAIL SPECIFICATIONS OF A 6000/SERIES 60 INTERFACE UNIT

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Prepared for

DEPUTY FOR COMMAND AND MANAGEMENT SYSTEMS
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Secure Front-End Processor/Central System Interface Unit Multiple Security Level Interface Channel List Processing

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This specification defines the technical requirements for an interface unit (IU) which connects a host central system to a secured front-end processor (SFEP). The IU transfers information across a single multiplexed channel according to IU command information contained in data control words. By using certified software resident in the central system and SFEP, the IU provides a method of handling multiple levels of security information. The IU provides a data format adapter (capable of binary or ASCII operation) which converts between

20. ABSTRACT (Continued)

a 36-bit central system word and a 16-bit SFEP word. An extended interface option is described which allows IU/central system interface lengths to be increased to 2000 feet.

PREFACE

Because of funding limitations, the Air Force terminated the effort which this document describes before the effort reached its logical conclusion. This specification has not been formally approved but was published in the interest of capturing and disseminating the computer security technology that was available when the effort was terminated.

This specification is published in two volumes. Volume I contains information that is suitable for public release. Volume II contains information that is proprietary and distribution is limited to U.S. Government agencies only. Other requests for Volume II of this document must be referred to H9 ESD (DRI) Hanscom AFB, Massachusetts, 01731.

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1.0 SCOPE

1.1 General

This specification defines the performance, design, development, and test requirements for a 6000/Series 60 Interface Unit (to be referred to as IU). The IU shall be used to provide an interface between a Secure Front-End Processor (SFEP) or Front-End Processor (FEP), which is a minicomputer of standard design, and a host central system. A selectable option to allow greater interface length between the FEP and central system is described in Paragraph 10 of this specification.

2.0 APPLICABLE DOCUMENTS

2.1 General Applicability

The following documents form a part of this specification to the extent specified herein. In the event of a conflict between the documents specified herein and the content of this specification, the contents of this specification shall be considered a superseding requirement.

2.2 Military Specifications and Standards

MIL-STD-454	Standard General Requirements for Electronic Equipment - Rev. D - 31 August 1973
MIL-STD-756	Reliability Prediction - Rev. A - 15 May 1963
MIL-STD-461A	Electromagnetic Interference - 1 August 1968
MIL-STD-1000	Drawings, Engineering, and Associated Lists

2.2 Military Specifications and Standards (Continued)

MIL-STD-1472	Human Engineering Design Criteria for Military Systems, Equipment, and Facilities - 15 May 1970
MIL-STD-130	Identification Markings of U.S. Military Property
MIL-HDBK-217B	Reliability, Stress and Failure Rate Data for Electronic Equipment
MIL-E-5400	General Specification for Aircraft Electronic Equipment
MIL-S-901C	Shock Test, High Impact, Shipboard Machinery, Equipment and System Requirements for (NAVY)
DCA Circular 370-D195-2	Test and Alterations, DCS Autodin TEMPEST Category II Testing
NACSEM 5100	Compromising Emanations Laboratory Test Standard Electromagnetic - October 1970
AFSC DH1-4	Electromagnetic Compatibility

2.3 Honeywell Documents

60126298	Engineering Product Specification for New Minicomputer Bus - Rev. C - 1 January 1975
58001102	Interface Specification, Direct Channel
FMS 40052	Florida Material Specification for Procurement, Inspection and Control of Raw Materials

2.3 Honeywell Documents (Continued)

FMS 40022	Florida Material Specification for Procurement, Inspection and Control of Raw Materials
FMS 40053	Florida Material Specification for Procurement, Inspection and Control of Raw Materials
FMS 40051	Florida Material Specification for Procurement, Inspection and Control of Raw Materials
FPS 18167	Florida Process Specification for Defining and Controlling Critical Processes
UED 23036	Workmanship Manual
ED 21618	Avionics Design Procedure
DS34025843	Detail Specification for a Security Protection Module
(TBS)	SFEP Subsystem Specification
(TBS)	Honeywell Ruggedized Level 6 (RL6) Reliability Program Plan
(TBS)	RL6 Integrated Logistics Support Plan

2.4 Other Documents

F19628-74-C-0205	Secure Communications Processor Architecture Study

3.0 REQUIREMENTS

The equipment specified herein shall be designed in accordance with the requirements of this specification. The IU design techniques specified in this document shall be subject to review by the customer.

3.1 Item Definition

This specification defines the 6000/Series 60 Interface Unit (IU) required to provide a data and control link between a Secure Front-End Processor (SFEP) and a host central system. In normal inter-computer transfer activities, the IU shall act as an agent of the SFEP which controls all detailed transactions. The IU shall respond to external stimuli from the SFEP and host central system. A stimulus from either system shall cause the IU to transfer information from one system to the other or interrupt either system.

The IU shall consist of SFEP/central system interfaces, registers to retain information during transactions, information path steering, parity checking and generation, configuration information, and control functions.

Unless otherwise indicated in this specification, references to the SFEP shall also apply to a FEP. The SFEP hardware will be implemented by including a Security Protection Module (SPM), as described in Detail Specification 34025843, into the FEP.

3.1.1 Item Diagram

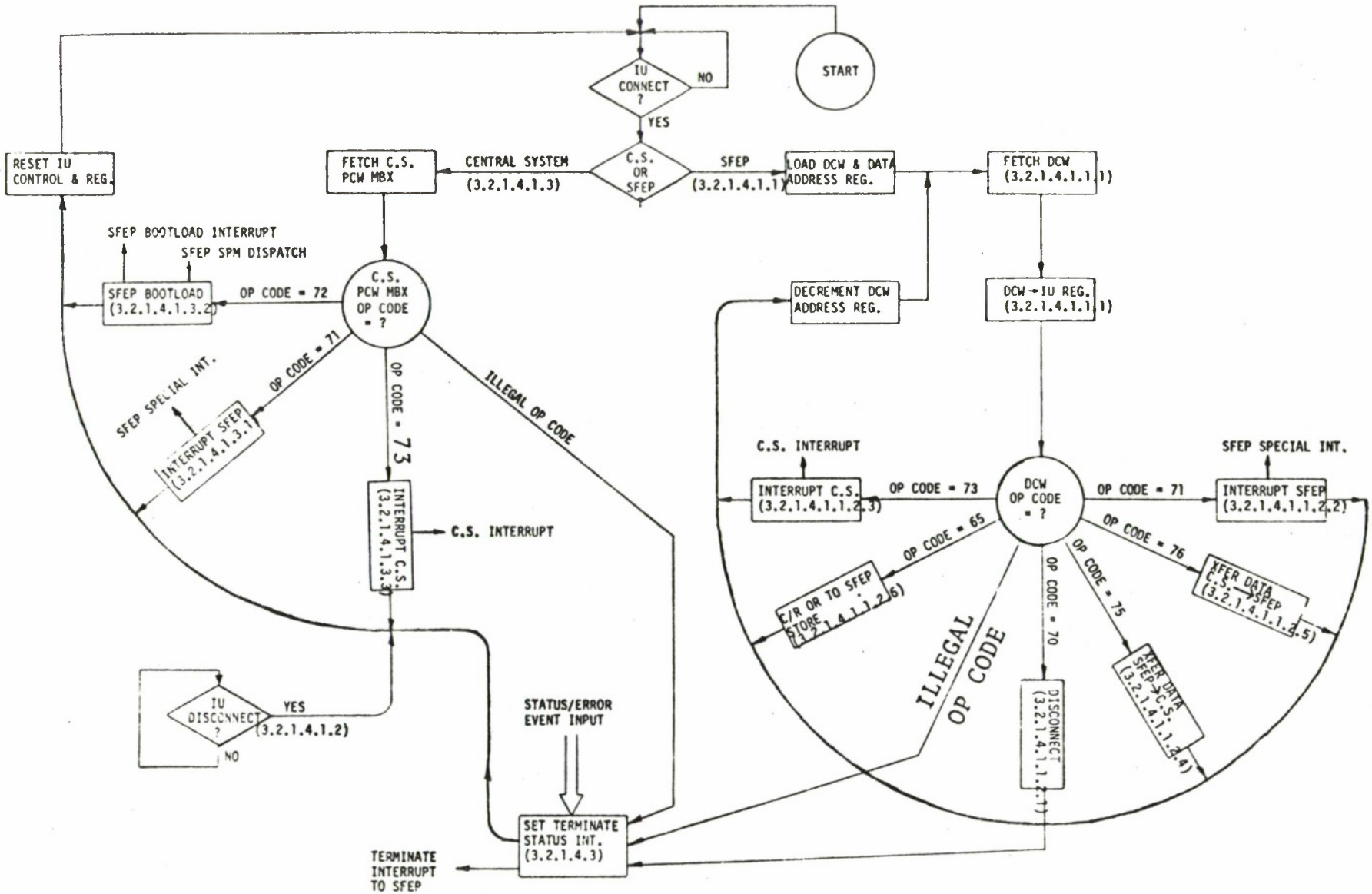
The IU functional diagram is shown in Figure 1. This figure illustrates the top level flow of the IU's essential functions. All numbers in this figure, enclosed in parentheses, refer to the paragraph in this document which describe the indicated IU operation and associated interaction of components within the IU.

3.1.2 Interface Definitions

The IU shall interface between a SFEP containing one or more processors and a central system as shown in Figure 2. The interface shown in Figure 2 indicates the IU interface for a single host and SFEP system configuration. The use of multiple IUs shall provide the interfacing capabilities for a single SFEP connected to multiple hosts. In the single host configuration, one IU will normally be used; however, if multiple IUs are needed, there will be multiple IOM/DCA (Direct Channel Adapter) interfaces required. For the multiple host configuration, there will be a minimum of one IU per host system. A single SFEP may support multiple IUs.

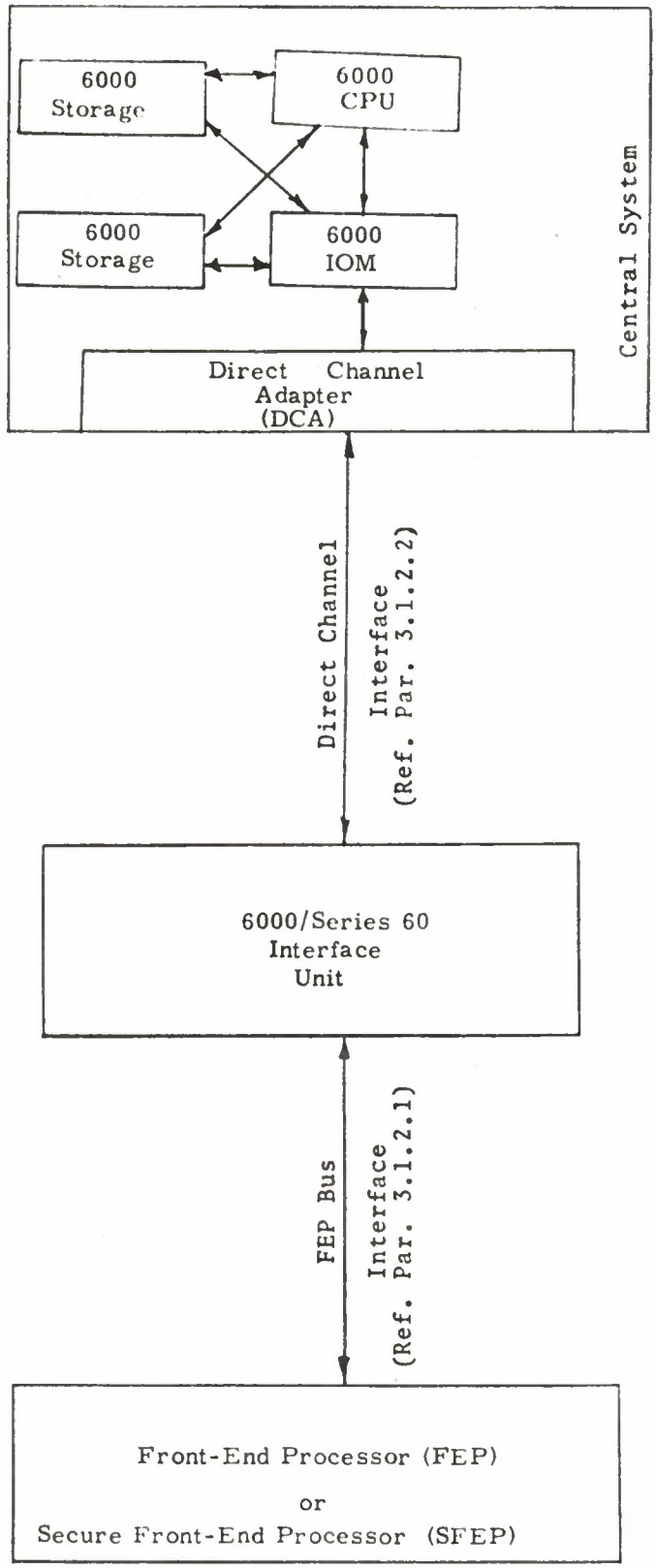
3.1.2.1 IU/SFEP Interface

The IU shall interface with the SFEP bus as defined in the Bus Specification 60126298, Rev. C. This bus contains address, data, timing, control, and miscellaneous signal information.



6000/SERIES 60 IU FUNCTIONAL DIAGRAM

Figure 1



6000/SERIES 60 IU INTERFACE

Figure 2

3.1.2.2 IU/Central System Interface

The IU shall interface with the central system as described in the Direct Channel Interface Specification 58001102. This bus contains control, status, and bi-directional information signals.

3.1.3 Major Component List

The following list identifies the major components which comprise the IU:

- Configuration Storage
- Address, Control, and Data Registers
- Information Path Steering
- Parity Checking and Generation
- Transfer Timer
- Control and Sequencer
- Format Adapter
- Terminate Interrupt Status Register
- Special Interrupt Cell Register

3.1.4 Government Furnished Property List

Government furnished property shall not be required.

3.1.5 Government Loaned Property List

Government loaned property shall not be required.

3.2 Characteristics

3.2.1 Performance

3.2.1.1 IU Capabilities

3.2.1.1.1 IU/Central System Data Transfer Rate

The IU/central system interface will dynamically adjust its transfer rates, without loss of information, according to the rate the information can be sent or received across the Direct Channel Interface. The maximum transfer rate which the IU/central system interface can support is a function of interconnect cable length and response time of the interface circuitry. The effects of the interconnect cable length and interface circuitry response time on the transfer can be determined as follows:

$$\text{Transfer Rate} = \frac{36 \text{ (bits per transfer)}}{4\ [t_d + t_r + t_c\ (L)]}$$

Where, t_d = 20 nsec max. (Direct channel interface transmitter propagation delay, generic P/N = DKLD1)

t_r = 20 nsec max. (Direct channel interface receiver propagation delay, generic P/N = DKLR1)

$t_c \simeq$ 2 nsec/ft (cable delay)

L = cable length (feet)

Transfer rate at maximum cable length of 75 feet = 47.4 MBPS.

The SFEP/central system throughput requirement shall be 10K characters/second (ref. SFEP Subsystem Specification).

3.2.1.1.2 Error Detection and Indication

The IU shall include provisions for detection and temporary storage of hardware parity errors associated with each of

3.2.1.1.2 Error Detection and Indication (Continued)

its interfaces and central system status errors (as described in the Direct Channel Specification 58001102). When an error is detected, the IU shall interrupt the FEP. See Paragraph 3.2.1.4.3 for a list of status events, including all such detected errors.

3.2.1.2 IU Security

The IU is implemented to be operated as a mapped or premapped SFEP I/O device. The selection of mapped or premapped operation is determined by a "SPM Flag Bit" (ref. DS 34025843) contained in address information supplied to the IU for accessing SFEP memory. The SPM Flag Bit shall be supplied to the IU during central system or SFEP "CONNECT" operations only and shall not be modified or used (except for addressing SFEP memory) by the IU during any other operations. Therefore, mapped or premapped operations are invisible to the IU. In the mapped mode, the IU references the SFEP memory with virtual addresses which are checked and absolutized within the SFEP. In the premapped mode, the IU references the SFEP memory with absolute addresses which have been premapped within the SFEP during the IU's "set-up" and "connect" commands (ref. Paragraph 3.2.1.4.1.1). A detailed explanation of mapped and premapped operation is contained in the Detail Specification for a Security Protection Module (DS 34025843).

For both mapped and premapped operations, the SFEP process issuing the IU's "connect" and "set-up" commands shall be

3.2.1.2 IU Security (Continued)

checked within the SFEP prior to IU I/O operations. When the IU is used with a non-secure front-end processor, the method of IU operations, as described in this document, is not affected. See Note 6.1 for additional discussion of IU usage for SFEP applications.

Since the IU provides a multiplexed channel which may carry information of multiple security levels, the IU's operations shall be controlled by certified software resident in the central system and SFEP.

3.2.1.3 Overview of Operation

3.2.1.3.1 List Processing

Refer to Volume II

3.2.1.3.2 Central System Initiated Commands

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3.2.1.4 Operational Characteristics

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3.2.1.4.1.1.1 Process DCW List

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3.2.1.4.1.1.2.3 Interrupt Central System (73)

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3.2.1.4.1.1.2.5 Data Transfer from Central System to SFEP (76)

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3.2.1.4.2 Data Formats

Refer to Volume II

3.2.1.4.3 Status/Error Events

Refer to Volume II

3.2.1.4.4 SFEP Program Interrupts

Refer to Volume II

3.2.2 Physical Characteristics

The IU is estimated to consist of one 15 by 16 inch rectangular circuit board. The board will be of multilayer or doublesided construction, on one inch centers, to be contained within a ruggedized cast chassis. In addition to the 15 by 16 inch rectangular circuit board, the IU shall also consist of one or more daughterboards.

The IU circuit board layout shall be implemented in a modular fashion to provide the capability of accommodating the extended interface option described in Paragraph 10.1.1. The extended interface shall be mechanized as an add-on or replacement function, either interfacing with the existing IU direct channel interface circuitry or completely replacing this circuitry with the interface circuits required by this option. For either case, the extended interface option shall be mechanized as a field selectable option without requiring modification to the IU circuitry. The exact method of the extended interface modular implementation shall be defined during the production IU board layout design.

3.2.2 Physical Characteristics (Continued)

In accordance with the specific program environmental confines, an option will be offered which will mechanically stiffen the boards as a means for ruggedization. In either case, the boards will be rail-mounted within the chassis. Electrical interface with the SFEP will be provided at the aft corners of the board via plug-in connectors. The weight of each board is estimated at between two to four pounds. Maintenance access will be from the front, after hinging of the front panel. The IU shall interface with the central system through connectors located on the back of the chassis.

The chassis which contains the IU shall be compatible with MIL-STD-461A electromagnetic requirements.

3.2.3 Reliability

Design considerations and parts selection shall be sufficient to assure that the equipment meets or exceeds its reliability requirements over its useful life.

3.2.3.1 Mean-Time-Between-Failures (MTBF)

The design goal calculated MTBF for the IU shall be greater than 20,000 hours. Calculations procedures shall be in accordance with MIL-STD-756 and Appendix A of MIL-HDBK-217B. Microcircuit failure rates to be employed in the calculations shall be as follows.

3.2.3.1 Mean-Time-Between-Failures (MTBF) (Continued)

IC Device Type	Failure Rate (Per 10^6 Hours)
SSI, less than 20 gates	0.03
MSI, 20 - 100 gates	0.05
LSI, greater than 100 gates	0.1
Bi-polar memory, RAM	0.3

3.2.3.2 Useful Life

The useful life of the IU shall be 10 years minimum when operated and maintained in accordance with the provisions of this specification.

3.2.4 Maintainability

Maintenance of the IU unit shall be effected by hinging of the chassis control panel and subsequently replacing any faulty or malfunctioning board with a spare board.

Faulty boards may then be returned to the manufacturer for detailed piece-part/circuit repair. This implies that the customer maintains an adequate stock of replacement spares.

Cost-effectiveness trade-offs have indicated that such a scheme, where the customer performs simple diagnostics to determine the faulty board for replacement, usually results in minimum service contract costs to the manufacturer.

3.2.5 Environmental Conditions

Temperature - The IU shall be operable within ambient temperatures ranging from 0°C to 50°C.

3.2.5 Environmental Conditions (Continued)

Vibration - For the IU within a hard-mounted chassis, the capability shall be sinusoidal vibration of 2.0 g's peak from 5 Hz to 2,000 Hz. When installed within an isolated chassis, the capability shall be extended to 10.0 g's peak from 5 Hz to 2,000 Hz.

Shock - The IU within an isolated chassis will be capable of withstanding a half-sine input pulse of 15.0 g's peak for a duration of 11.0 milliseconds. In an isolated unit, the IU shall be capable of withstanding pulses in accordance with MIL-S-901C, for lightweight equipment.

Altitude - The IU shall be required to satisfactorily operate from 0 to 8,000 feet altitude.

Humidity - The IU must satisfactorily withstand a relative humidity of 100 percent.

3.2.6 Transportability

Each board of the IU shall be suitably packaged in its own protective container. Several boards may be shipped in the same container, provided that such is partitioned between component boards and that each board is individually foam-packed. Packing shall be sufficient to prevent damage to a board or board components in the event that the overall transportation container becomes damaged.

3.3 Design and Construction

3.3.1 Materials, Processes, and Parts

Materials, parts, and processes shall conform to the requirements of MIL-E-5400 when practical or unless otherwise restricted herein. Design and application considerations, as well as economic factors, shall govern the selection of and use of materials, parts, and processes. Honeywell Information Systems (HIS) materials, parts, processes, and controlling specifications used for the existing Level 6 minicomputer design and Avionics FMSs and FPSs used for the IU design shall be considered approved for the IU upon verification of data substantiating that the unit will perform satisfactorily in the specified environment. In addition, the following paragraphs identify specific requirements and limitations in the use of materials, parts, and processes.

3.3.1.1 Elastomeric Materials

Elastomeric components shall utilize only those elastomers which have adequate resistance to aging, ozone, heat aging, low temperature embrittlement, and reversion, either temperature or moisture-temperature induced.

3.3.1.2 Wire

Wire used in the IU design shall conform to the following specifications:

- 300V, Single Conductor - FMS 40052
- 300V, Shielded - FMS 40022

3.3.1.2 Wire (Continued)

- 600V, Single Conductor - FMS 40053
- 600V, Shielded - FMS 40051

3.3.1.3 Conformal Coatings

Printed circuit cards shall be conformally coated per FPS 18035, Type V.

3.3.1.4 Soldering

Electrical soldering practices shall be in accordance with FPS 18167. Certification of soldering operators is required.

3.3.1.5 Parts Selection and Standardization

Electronic part types for all new IU circuit designs shall be selected from Honeywell's Boston Computer Operations (BCO) Standard Parts List. Selection, qualification, and screening criteria applicable to nonstandard parts shall be in accordance with Parts Control Program Requirements of the Honeywell Ruggedized Level 6 (RL6) Reliability Program Plan.

3.3.2 Electromagnetic Radiation

The IU shall be designed in accordance with the guidelines contained within AFSC DH 1-4, Electromagnetic Compatibility.

3.3.2.1 EMC

Electromagnetic compatibility criteria for the IU when housed in the RL6 chassis shall be in accordance with the emissions and susceptibility test requirements of MIL-STD-461A, Notice 3,

3.3.2.1 EMC (Continued)

1 May 1970 for Class A3 equipment. Applicable requirements are:

- CE03 - Conducted Emissions, power lines
- CE04 - Conducted Emissions, signal lines
- CS01 - Conducted Suscept, power lines, AF
- CS02 - Conducted Suscept, power lines, RF
- CS06 - Conducted Suscept, power lines, transient
- RE02 - Radiated Emissions, electric field
- RS03 - Radiated Suscept, magnetic induction field
- RS03 - Radiated Suscept, electric field

3.3.2.2 TEMPEST

TEMPEST criteria for the IU when housed in the RL6 chassis shall be in accordance with the following portions of NACSEM 5100 as specified by DCA Circular 370-D195-2:

- Electric Field Space Radiated
- Power Line Conduction
- Black Signal Line Conduction
- Red Signal Line Conduction

3.3.3 Identification and Marking

Identification and marking for Avionics designed hardware shall be in accordance with MIL-STD-130. Identification and marking for BCO designed hardware shall be per BCO standards. If existing designs do not meet these requirements, it shall be documented and corrective action shall be taken if necessary.

3.3.4 Workmanship

Workmanship of the IU shall be in accordance with the applicable portions of UED 23036. General workmanship shall be of high quality to assure compliance with specification requirements including the service life requirement.

3.3.5 Interchangeability

3.3.5.1 General

Mechanical and electrical interchangeability shall exist between like assemblies, subassemblies, and replaceable parts regardless of manufacturer or supplier. Interchangeability, as used here, does not mean identity, but requires that a substitute of like assemblies, subassemblies and replaceable parts may be easily effected without physical or electrical modifications to any part of the equipment or assemblies including cabling, wiring, and mounting.

3.3.5.2 Module Interchangeability

IUs or like modules within an IU shall be replaceable and interchangeable without electrical adjustment or calibration. A mechanical adjustment of the IU channel number switch may be required.

3.3.6 Safety

The IU shall be designed to combine maximum safety and stability, avoiding sharp edges, protrusions, obstructions and any other mechanical or physical features which constitute a hazard in accordance with MIL-STD-1472, Sections 4.13.4 and 5.13.5.

3.3.7 Human Performance/Human Engineering

There shall be no human engineering or performance requirements associated with the IU.

3.4 Documentation

3.4.1 Drawings

All Avionics engineering released drawings shall be equivalent to or better than that required by MIL-STD-1000, Category E, Form 3. BCO drawings shall conform to HIS Standards.

3.4.2 Specification

Specifications are required for all parts, materials, and processes utilized in the fabrication and assembly of this unit. This requirement is necessary to assure the validity of Qualification Test Results.

3.4.3 Test Plans

Test plans shall be per Avionics Design Procedures, Paragraph 5.3.

3.5 Logistics

Maintenance procedures, supplies, facilities, facility equipment, personnel, and training requirements shall be per the approved RL6 Integrated Logistics Support Plan.

3.6 Personnel and Training

There are no personnel and training requirements relating to the IU.

3.7 Major Component Characteristics

3.7.1 Configuration Storage

Refer to Volume II

3.7.1.1 IU Device Identification Number

Refer to Volume II

3.7.1.2 DBR Address

Refer to Volume II

3.7.1.3 Central System Mailbox Address

Refer to Volume II

3.7.1.4 SFEP SPM Channel Number

Refer to Volume II

3.7.1.5 SFEP Bootload Interrupt Level

Refer to Volume II

3.7.1.6 Central System Emergency Interrupt Level

Refer to Volume II

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3.7.1.7.1 IU Channel Number 1

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3.7.2.2 SFEP Data Address Register

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3.7.2.4 Tally Register

Refer to Volume II

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Refer to Volume II

3.7.7 Format Adapter

Refer to Volume II

3.7.8 Terminate Interrupt Status Register

Refer to Volume II

3.7.9 Special Interrupt Cell Register

Refer to Volume II

4.0 QUALITY ASSURANCE PROVISIONS

4.1 General

The Quality Assurance Program to be applied to the IU shall be conducted in accordance with the criteria described herein and the SCOMP Product Assurance Program Plan. The

4.1 General (Continued)

SCOMP PA Program Plan shall describe the integrated quality and reliability and security verification activities applicable to IU prototype and production systems.

4.1.1 Responsibility for Tests

Unless otherwise specified in procurement documentation, the supplier is responsible for the performance of all tests and inspections specified herein.

4.1.2 Special Tests and Examinations

The requirements of Sections 3.0 shall be verified entirely, or in part, by inspection of the equipment and its drawings.

A. (3.2.2) Physical Characteristics

B. (3.3.3) Identification and Marking

C. (3.3.4) Workmanship

D. (3.3.5) Interchangeability

4.1.3 Reliability Analysis

See Paragraph 3.2.3.

4.2 Quality Conformance Inspections

4.2.1 Engineering Design Evaluation

4.2.1.1 Prototype Development Tests

A prototype IU shall be subjected to design evaluation test sequences to verify its functionality and operation under worst case conditions of power, temperature, and clock frequency operation. The tests shall be conducted with the

4.2.1.1 Prototype Development Tests (Continued)

IU installed in a minicomputer configuration whose functional elements have been previously acceptance tested.

Final prototype development tests shall be conducted with the IU and SFEP integrated with a host central system.

4.2.1.2 Prototype Test Software

A prototype IU-SFEP shall be developed and tested using evaluation software developed with the aid of an Interface Wrap-around Test Unit. The software developed in this configuration shall test the IU to assure the electrical performance requirements, described in Paragraph 3.0, are exercised.

4.2.1.3 IU Qualification Tests

Environmental qualification tests for the IU are not required. Qualification for the IU shall be established by structural similarity to ruggedized minicomputer circuit elements upo- which tests shall be performed. The similarity units shall include at least one CPU and one 32K word memory.

4.2.2 Prototype Inspection and Test

Prototype subassemblies shall be visually inspected for workmanship, damage and assembly configuration prior to first powered operation. Prototype IUs shall be acceptance tested in accordance with Paragraph 4.2.1.1.

4.2.3 Production Acceptance Tests and Inspections

4.2.3.1 Inspection Criteria

4.2.3.1.1 Workmanship

Workmanship shall be verified on each production IU to Honeywell workmanship standard, UED 23036, to meet the requirement of MIL-STD-454, Requirement 9.

4.2.3.1.2 Configuration

Each production IU shall be visually examined in individual parts kit form prior to issuance to assembly and again upon completion prior to acceptance testing. Configuration examination shall include:

- Verification that correct part types have been issued for manufacture.
- Completed assemblies are complete and visually identical to a standard reference IU or photograph thereof.

4.2.3.1.3 Electronic Parts Inspection

The logic functionality damage and marking of integrated circuits to be assembled into production IUs shall be verified by inspection and test prior to assembly. Appropriate quality control control sampling plans based lot total percent defective (LTPD) acceptance criteria shall be employed for marking and damage.

4.2.3.2 Production Acceptance Testing

4.2.3.2.1 Acceptance Tests

Production acceptance tests shall be conducted under the supervision of quality control using approved test procedures, equipment and software. Each IU shall be accepted with the SFEP (or FEP) unit for which it is intended. Spare IUs may be acceptance tested in any SFEP (or FEP) of compatible configuration provided that all functional elements used in the test have been inspected in accordance with Paragraph 4.2.3.1. The final acceptance of the IU shall be predicated upon the successful integration of the IU and SFEP (or FEP) with a host central system.

4.2.3.2.2 Production Test Software

Software used for acceptance testing of production IUs shall be derived from the prototype software (see Paragraph 4.2.1.2) or other suitable source which ensures that each IU function is exercised.

Production test software shall be formally issued and controlled by quality assurance in accordance with Honeywell Design Procedure 3.3.

5.0 PREPARATION FOR DELIVERY

See Paragraph 3.2.6.

6.0 NOTES

6.1 Security Notes

The IU's implementation provides for software flexibility in selecting mapped or premapped operation with IU or SPM hardware modification. The two I/O commands ("set-up" and "connect" described in Paragraph 3.2.1.4.1.1) required to initiate IU activity from the SFEP define the starting locations of a DCW list and a data buffer area in the SFEP memory. In addition, each I/O command has a unique device identification number associated with it, which enables the SPM to simultaneously retain descriptors required for the IU to access DCW and data buffer locations in separate areas of memory. This eliminates any requirements of constructing a DCW list and a data buffer in a single logically contiguous area of secured memory space.

The mechanization of the IU for SFEP applications does not support general scatter/gather operations (although logically contiguous areas of SFEP memory may be physically scattered). However, in practice, this limitation is not a real constraint since each IU "connect" usually covers a data transfer for only a single user terminal.

6.2 Read, Clear, OR, and Restore Central System Note

The "Read, Clear, OR, and Restore Central System" op, contained in a DCW (reference Paragraph 3.2.1.4.1.1.2.6), is utilized to provide a synchronous means of the SFEP/IU

6.2 Read, Clear, OR, and Restore Central System Note (Continued) updating a Terminate Interrupt Multiplex Word (TIMW) normally resident in the central system's header mailbox area. The Read and Clear portion of this operation performs the function of transferring the TIMW to the IU while zeroing the TIMW contents in the central system. To achieve synchronization between the central system and SFEP, a zero state of bit 35 is used to indicate to the central system that the TIMW is in process of being updated by ghe SFEP/IU. The OR and Restore performs the actual update of the TIMW.

Typically, when the SFEP is told to read a particular channel mailbox, the central system is required to wait until the SFEP is finished with the mailbox area before it can be reused. Once the SFEP is finished with the mailbox, it performs the "Read, Clear, OR, and Restore" operation on the TIMW (ORing the bit which corresponds to the mailbox being released) then interrupts the central system (reference Paragraph 3.2.1.4.1.1.2.3). Upon receiving the interrupt, the central system looks at the TIMW and interprets the TIMW set bit as a mailbox area available for future use.

6.3 Format Adapter Notes

6.3.1 Binary and ASCII/Tally Count Relationships

As discussed in Paragraph 3.2.1.4.2, binary or ASCII transfers between the central system and SFEP can end on in exact multiples of their respective packing ratios. The IU shall be implemented to pack/unpack SFEP words, as

6.3.1 Binary and ASCII/Tally Count Relationships (Continued)

described in Paragraph 3.2.1.4.2, in a sequence based entirely on the tally count (number of 36-bit words to be transferred) and format mode. Therefore, transfers can access SFEP memory beyond the actual data area. For each transfer, the amount of overlap can be determined by the sender from the known words to be transferred, tally count required for the transfer, and format mode of operation. From this information, the number of unused bits (if any) of the last word to be transferred can be communicated with the receiving system via a channel mailbox transfer normally occurring prior to the transmission of user buffer information. A 5-bit field of the channel mailbox would be sufficient to encode the maximum number of possible unused bits (32) for any transfer. The transfer of each channel mailbox area (8, 36-bit words) would not require "unused bit compensation" since they are exact multiples for both ASCII and binary formats.

6.3.2 BDC to ASCII Conversion Considerations

BDC to ASCII format conversion shall not be performed by the IU hardware. If this feature were to be incorporated into the hardware with the present binary/ASCII capability maintained, the DCWs format adapter information would be required to increase from a 1 to 2 bit field.

10.0 APPENDIX I

10.1 Direct Channel Interface Extension Option

The IU/central system direct channel interface is constrained to a length of ≤ 75 feet. The capability to implement an extended interface between the IU and central system shall be provided in the IU design. This option will allow the interface length to be increased to ≤ 2000 feet. Data transfer rates will be degraded according to the extended cable lengths and propagation delays of the additional interface elements described in Paragraphs 10.1.1 and 10.1.2. The design of the extended interface option shall be defined at the completion of the IU prototype design. Figure 8 illustrates how this option would be implemented.

10.1.1 IU Extended Interface

The IU's enclosure shall provide sufficient space to incorporate a special interface board consisting of line driver and receiver elements (see Paragraph 3.2.2 for the physical mechanization of this board). These interface elements shall allow the special board to interface with the present IU and provide a differential interface for transmitting and receiving signals across the extended interface length. The extended interface elements shall have electrical characteristics similar to the National Semiconductor Corp. device P/N 8820 (receiver) and 8831 (driver).

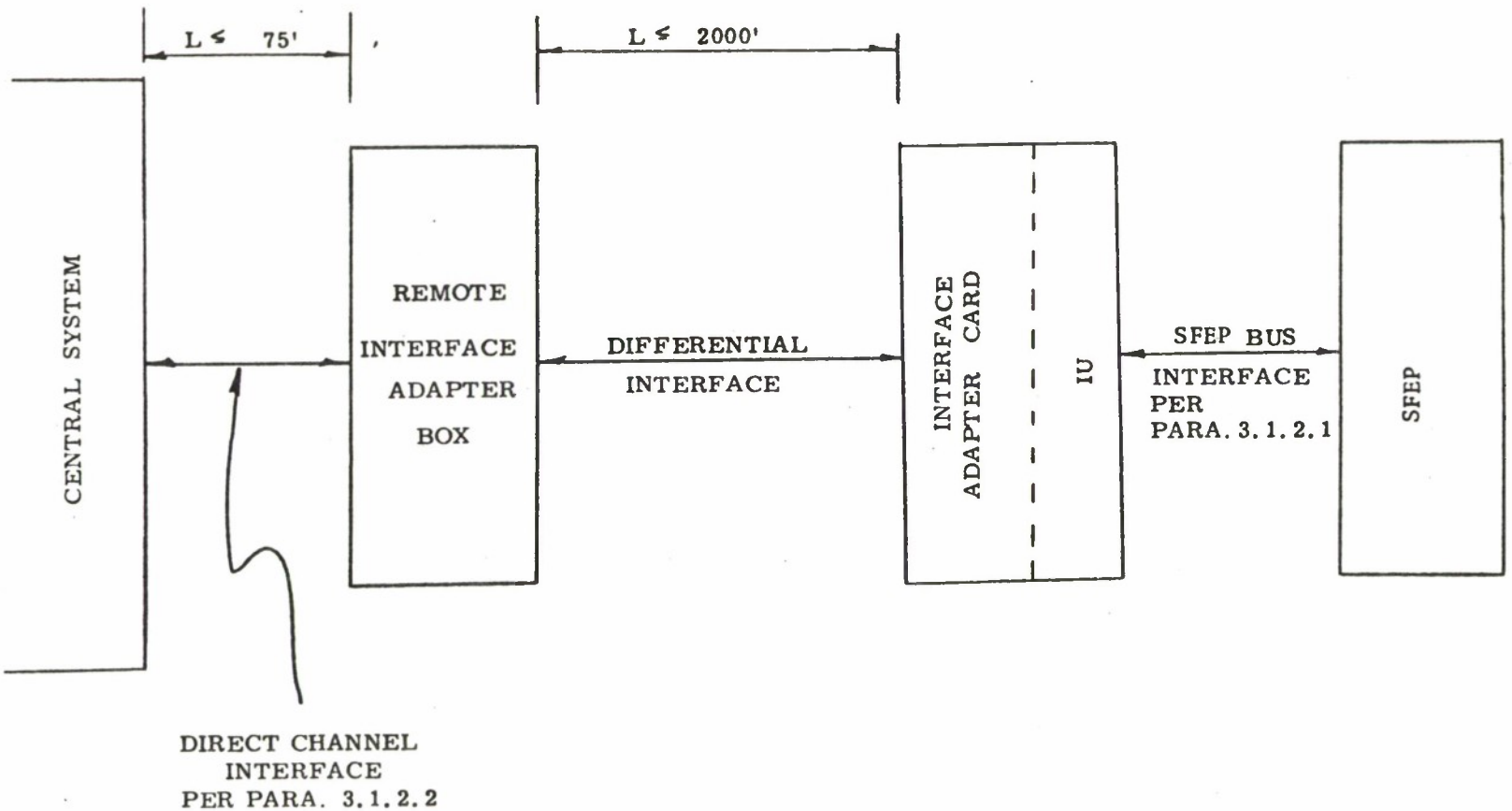

DIAGRAM OF OPTIONAL INTERFACE EXTENSION

Figure 8